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EXAMINER	
SONG, JASMINE	
ART UNIT	**PAPER NUMBER**
2188	03

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,252	STAFFORD, WILLIAM R.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-24 and 26-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-24 and 26-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This office action is in response to Amendment H filed on 12/22/2003, paper #22, which canceled claims 25, 39-41. Claims 19-24, 26-38 are therefore still pending. All rejections and objections not explicitly repeated below are withdrawn.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

3. The rejections of claims 19-24, 26-38 are maintained under 35 USC § 103 as shown below.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 19-21,23-24 and 26-29,32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloud et al., U.S. Patent 5815427, in view of Tremblay., U.S. Patent 6021469.

Regarding claims 19, 26,32 and 39, Cloud et al. teach a memory device (Fig.1 and 7, element 10) coupled with the processor (Fig.7, element 84), the memory device (Fig.1, element 10) comprising memory storage (Fig.1, element 12) and three different interfaces (Fig.1, element 14 includes three different interfaces which are shown in the Fig.5 and 6) such as the programming interface (Fig.5, col.5, lines 45-58), the test interface (Fig.6, element 77, col.6, lines 44-47) and operation interface (Fig.6, element 74 and 76, col.6, lines 36-44) to operate the memory storage (Fig.1, element 10) in at least one of three different modes (Fig.5 and 6, col.5, lines 45-58 and col.6, lines 36-47), the test interface to test the memory device (Fig.6, element 77, col.6, lines 44-47). the programming interface to program the memory storage (Fig.5, col.5, lines 45-58).

Cloud does not teach that the memory storage and the three different interfaces reside in a common die.

However, Tremblay teaches that a memory storage (it is taught as external memory which does not show in Fig.1, normally means main memory) and three different interfaces (three interfaces: I/O controller interfaces 111, memory controller interfaces 112 and instruction cache unit interface 120 or three interfaces: I/O controller interfaces 111, memory controller interfaces 112 and data cache unit interface 160; col.11, lines 23-35 and col.17, lines 44-45) reside in a common die (Fig.1, element 100, hardware processor) (col.11, lines 27-28 and 32-34).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Tremblay in the memory system of Cloud and have the memory storage and the three different interfaces reside in a common die for the advantage of much better performance characteristics (col.5, lines 40-42 and col.6, lines 3-5) and not necessarily to arbitrate to use the memory bus since the memory storage and the three different interfaces as hardware processor is the only master (col.11, lines 27-28 and 39-41).

According, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantage set forth above.

Regarding claims 20, 27 and 33, Cloud et al. teach that selection circuitry (Fig.6, element 62) to select among the three different interfaces (Fig.5 and 6, col.5, lines 45-58 and col.6, lines 36-47).

Regarding claims 21, 29, 35, Cloud et al. teach that the three different interfaces comprises:

a test interface to test the memory device for defects (Fig.6, element 77, col.6, lines 44-47).

a programming interface to program the memory device with a code (Fig.5, col.5, lines 45-58).

an operation interface to operate the memory device in an operation mode (Fig.6, element 74 and 76, col.6, lines 36-44).

Regarding claims 24-25, 28 and 34, Cloud et al. teach that the selection circuitry comprises:

a plurality of drivers (col.2, lines 45-48), each of the plurality of drivers coupled between a device pad and a device circuit (col.3, lines 1-32), each of the plurality of drivers having a control input (Fig.6) and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers (Fig.5, element 57, col.5, lines 22-45).

Regarding claim 23, Cloud et al. teach the operation interface is a proprietary interface (col.6, lines 36-44col.5, lines 56-65).

Regarding claim 40, Cloud et al. teaches that selecting the programming interface and wherein operating comprises programming the memory device with code using the programming interface (col.5, lines 39-60)

Regarding claim 41, Cloud et al. teaches that selecting the test interface and wherein operating comprises testing the memory device for defects using the test interface (col.6, lines 44-47).

6. Claims 22, 30-31 and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloud et al., U.S. Patent 5815427.

Regarding claims 22, 30-31 and 36-38, Cloud et al. teach the limitations in the claims above. Cloud does not teach the memory device is a flash memory and BIOS memory. However, Cloud indicates that the memory device is SDRAM, but it may be another type of memory device (col.6, lines 3-7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the memory device as the BIOSs which store on a flash memory chip that can be upgraded via software. This would have motivated one of ordinary skill in the art to use flash memory chip in a PC so that the BIOS could be updated in place instead of being replaced.

Response to applicant's Arguments

7. Applicant's arguments filed 12/22/2003 have been fully considered but they are not persuasive.

8. In response to applicant's argument that the memory controller interface 112 is not used to operate instruction cache 125. Rather, memory controller interface 112 is used to interface data cache 165 with an external memory (see applicant's remarks on page 8), the examiner agrees that the memory controller interface 112 is not used to operate instruction cache 125, however, three interfaces: I/O controller interfaces 111, memory controller interfaces 112 and instruction cache unit interface 120 or three interfaces: I/O controller interfaces 111, memory controller interfaces 112 and data

cache unit interface 160 of Tremblay and memory storage (the external memory) of Tremblay reside in a common die (hardware processor 100, col.11, lines 32-34), and the three interfaces as noted above are used to operate the external memory as shown in Fig.1.

9. In response to applicant's argument that Tremblay teaches away from combination with Cloud because Tremblay teaches away from the use of additional on die memory storage (see applicant's remarks on page 8 to page 9), the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Tremblay teaches that a memory storage (it is taught as external memory which does not show in Fig.1, normally means main memory) and three different interfaces (three interfaces: I/O controller interfaces 111, memory controller interfaces 112 and instruction cache unit interface 120 or three interfaces: I/O controller interfaces 111, memory controller interfaces 112 and data cache unit interface 160; col.11, lines 23-35 and col.17, lines 44-45) reside in a common die (Fig.1, element 100, hardware processor) (col.11, lines 27-28 and 32-34) for the advantage of much better performance characteristics (col.5, lines 40-42 and col.6, lines 3-5) and not necessarily to arbitrate to use the memory bus since the memory

storage and the three different interfaces as hardware processor is the only master (col.11, lines 27-28 and 39-41), therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize or modify the teachings of Tremblay in the memory system of Cloud and have the memory storage and the three different interfaces reside in a common die for the advantages as noted above.

10. In response to applicant's argument that Could teaches away from the use of a flash memory device and therefore, there is no motivation to combine the cited references (see applicant's remarks on page 9 for claim 38), the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Cloud discloses inexpensive volatile memory device SDRAM that lose their stored data when power to the memory is removed, the Examiner agrees that cost effectiveness is one of the problems confronting the inventors of Cloud and advantages of the teachings of Cloud, however, Cloud clearly indicates that another type of memory device can be used (col.6, lines 3-7), other type of memory device include the flash memory since the flash memory have the advantage of keeping the content of data stored even the power to the memory is off, this advantage is taught in

the Yamada's reference, U.S. Patent 6125423 (col.1, lines 19-23), as one may noted above, "obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art", the motivation of using SDRAM (cost effectiveness) can be different than the motivation of using flash memory (keeping the content of data stored even the power to the memory is off), therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the flash memory device instead of SDRAM for the advantage as noted above.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-5:30 (first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song
Patent Examiner
March 19, 2004

Mano Padmanabhan 3/19/04
Supervisory Patent Examiner
Technology Center 2100